CLAIMS

What is claimed is:

1. A method for providing data for sample rate conversion, the method comprises the steps of:

generating a data request interrupt based on a system clock and a sample rate conversion value;

receiving a data ready control signal from a data processor;

responding to the data request interrupt by providing a read signal to a temporary memory device, wherein a first word of the data is read from the temporary memory device and provided to a sample rate conversion module; and

responding to the data ready control signal by providing a write signal to the temporary memory device, wherein a second word of the data is written to the temporary memory device by the data processor.

2. The method of claim 1 further comprises:

determining the sample rate conversion value based on the system clock and a data clock.

3. The method of claim 1, wherein the generating a data request interrupt further comprises:

repetitively generating subsequent data request interrupts based on the system clock and the sample rate conversion value, such that a series of words are read from the temporary memory.

4. The method of claim 1, wherein the receiving the data ready control signal further comprises:

receiving a plurality of data ready control signals at a rate of data, wherein the rate of data is based on sample rate of xDSL data.

5. The method of claim 1 further comprises:

generating a second data request interrupt based on the system clock and a second sample rate conversion value;

receiving a second data ready control signal from a second data processor;

responding to the second data request interrupt by providing a read signal to a second temporary memory device, wherein a first word of the second data is read from the second temporary memory device and provided to a second sample rate conversion module; and

responding to the second data ready control signal by providing a write signal to the second temporary memory device, wherein a second word of the second data is written to the second temporary memory device by the second data processor.

6. An apparatus for providing data for sample rate conversion, the apparatus comprises:

a data processor operable to receive input data and to produce formatted data at a data clock rate;

temporary memory device; and

sample rate interface module operably coupled to obtain a system clock and a sample rate conversion value and is operably coupled to receive a data ready control signal from the data processor, wherein the sample rate interface module provides a read signal to the temporary memory device such that a first word of formatted data is read from the temporary memory device and provided to a sample rate conversion module, wherein, in response to the data ready control signal, the sample rate interface module provides a write signal to the temporary memory device, wherein a second word of the formatted data is written to the temporary memory device by the data processor, and wherein the read signal is generated based on the system clock and the sample rate conversion value.

7. The apparatus of claim 6 further comprises:

a value module operably coupled to produce the sample rate conversion value based on a function of the system clock and the data clock rate, wherein a resultant of the function is the sample rate conversion value.

8. The apparatus of claim 6 further comprises:

a second data processor operable to receive second input data and to produce second formatted data at a second data clock rate; and

second temporary memory device, wherein the sample rate interface module provides a second read signal to the second temporary memory device such that a first word of second formatted data is read from the second temporary memory device and provided to a second sample rate conversion module, wherein, in response to the second data ready control signal, the sample rate interface module provides a second write signal to the second temporary memory device, wherein a second word of the second formatted data is written to the second temporary memory device by the second data processor.

9. An apparatus for providing data for sample rate conversion, the apparatus comprises:

a data processor operable to receive input data and to produce formatted data at a data clock rate;

temporary memory device; and

sample rate interface module operably coupled to obtain a system clock and a sample rate conversion value, wherein the sample rate interface module provides a read signal to the temporary memory device such that a first word of the input data is read from the temporary memory device and provided to the data processor, wherein the sample rate interface module provides a write signal to the temporary memory device such that a second word of the input data is written to the temporary memory device, wherein the read signal is generated based on the system clock and the sample rate conversion value.

10. The apparatus of claim 9 further comprises:

a value module operably coupled to produce the sample rate conversion value based on a function of the system clock and the data clock rate, wherein a resultant of the function is the sample rate conversion value.

11. An apparatus for providing data for sample rate conversion, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

generate a data request interrupt based on a system clock and a sample rate conversion value;

receive a data ready control signal from a data processor;

respond to the data request interrupt by providing a read signal to a temporary memory device, wherein a first word of the data is read from the temporary memory device and provided to a sample rate conversion module; and

respond to the data ready control signal by providing a write signal to the temporary memory device, wherein a second word of the data is written to the temporary memory device by the data processor.

12. The apparatus of claim 11, wherein the memory further comprises operational instructions that cause the processing module to:

determine the sample rate conversion value based on the system clock and a data clock.

13. The apparatus of claim 11, wherein the memory further comprises operational instructions that cause the processing module to generate a data request interrupt by:

repetitively generating subsequent data request interrupts based on the system clock and the sample rate conversion value, such that a series of words are read from the temporary memory.

14. The apparatus of claim 11, wherein the memory further comprises operational instructions that cause the processing module to receive the data ready control signal by:

receiving a plurality of data ready control signals at a rate of data, wherein the rate of data is based on sample rate of xDSL data.

15. The apparatus of claim 11, wherein the memory further comprises operational instructions that cause the processing module to:

generate a second data request interrupt based on the system clock and a second sample rate conversion value;

receive a second data ready control signal from a second data processor;

respond to the second data request interrupt by providing a read signal to a second temporary memory device, wherein a first word of the second data is read from the second

temporary memory device and provided to a second sample rate conversion module; and

respond to the second data ready control signal by providing a write signal to the second temporary memory device, wherein a second word of the second data is written to the second temporary memory device by the second data processor.